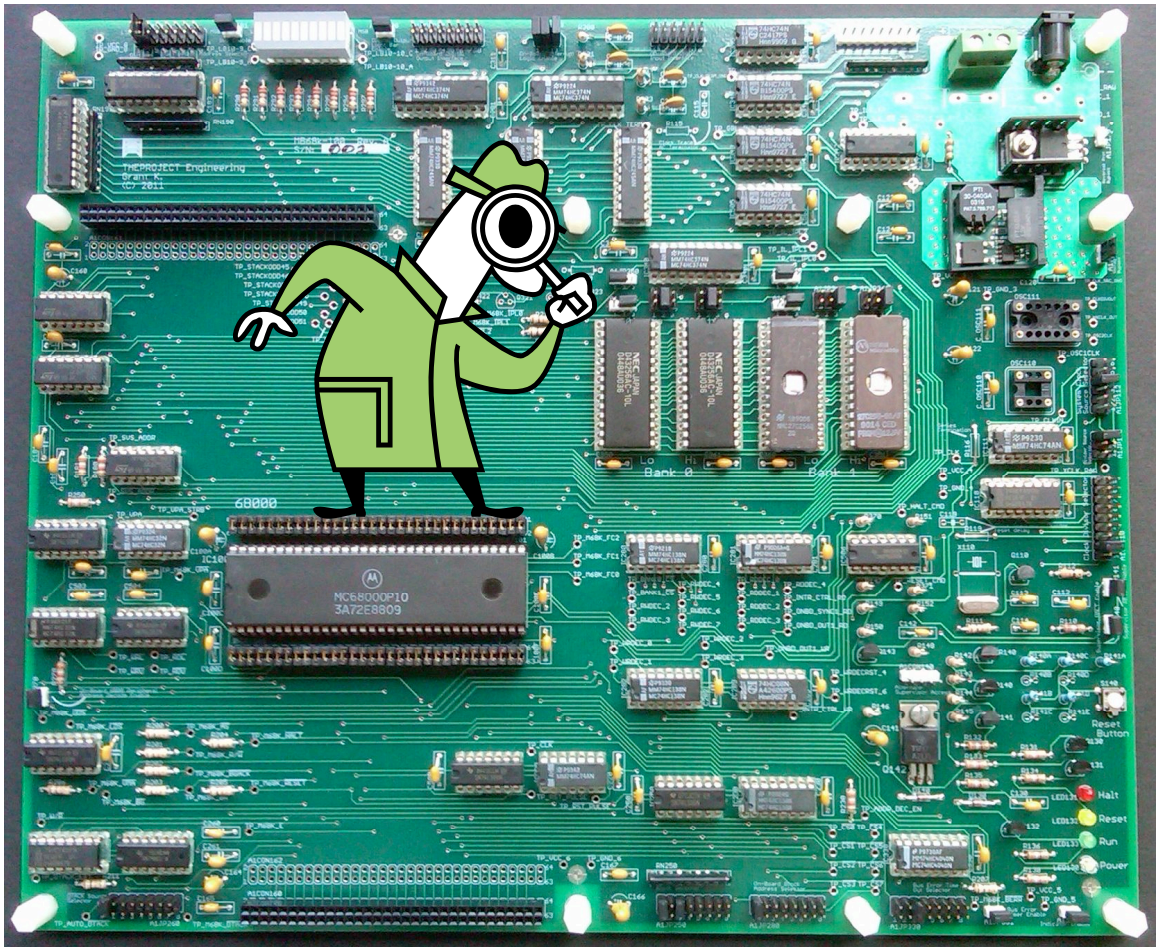
MB68k-100 Motherboard Test Procedure, C

Set Up Instructions:

- ✓ DC power supply
- ✓ Obtain 2 solid core jumper wires for testing
  - 1’ length for “pull-up” wire, installing one end in A1CON161, pos 61
  - 2” length for /DTACK loop back

- ✓ Connect MOS 6581 sound system as indicated in Appendix A for 6800 support test
- ✓ Install 2 program EPROM chips in Bank 0 with TstExamp test software (v1.0.x)
  - The primary purpose of this application is to facilitate easy test of the MB68k-100 hardware. Using simple inputs, much of the MB68k-100 circuitry is exercised and the results are displayed.
- ✓ Install 2 1k x 8 SRAM chips in Bank 1 (sized to support stack)
- ✓ Install On-Board Output Latch light bar, DZ290
- ✓ Install SVS A1JP180, position 2 for Bank 0 execution from program EPROM
- ✓ Install jumpers Auto /DTACK, A1JP250, for CS0 (On-Board) & CS7 (FPGA)
- ✓ Otherwise use default jumper selections



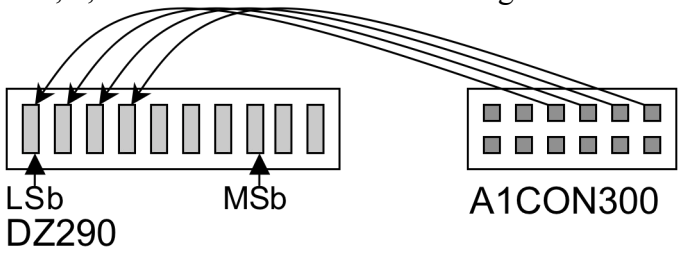
Revision History:

Revision	Date	Description
A	11/20/11	• Initial
B	12/04/11	• Improved Hardware Entropy Generator test with TstExamp v1.0.1 • Revised document name
C	12/18/11	• Removed third (bug fix) identifier from software revision in 'Set Up Instructions' • Elaborated System Fault Traps to capture and report system faults in Troubleshooting section

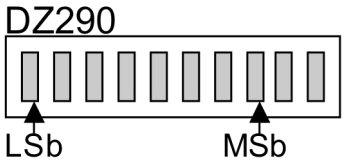
Test Procedure:

Test sequence requires about 15 minutes.

Step Number	Test Step	Test Criteria
1	Apply Power	
1.1	Apply input power to MB68k-100. This may be done by applying +5VDC via A1TB120.	Verify that, • Input Power < 2.2W • Power, LED130 – White
2	Verify Power On Reset	
2.1	Verify that the Halt and Reset LEDs initially illuminate with applied power for approximately 2 seconds. During this, verify the Run LED is not illuminated.	For about 3 seconds, • Halt, LED131 – Red • Reset, LED132 – Yellow • Run, LED133 – Off
2.2	Verify that the Halt and Reset LEDs turn off after the initial 2 second period on.	After the 3 seconds, • Halt, LED131 – Off • Reset, LED132 – Off
3	Program Run	
3.1	Wait for the Power On Reset operation to complete.	Verify the green Run LED illuminates.

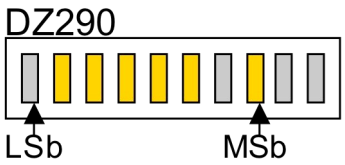
4	On-Board Register Initialization On start-up, the initial states of the writable on-board registers are displayed on the On-Board Output Latch. These registers are the Interrupt Enable and On-Board Output Latch. Both should initialize to zero. The output cycles between displaying their initial values respectively. It briefly sweeps a single LED position across the output during the transition. To select another test mode at any time, pull the corresponding interrupt trigger level bit high.	
4.1	--	Verify the On-Board Output Latch light bar, DZ290, displays a single illuminated LED in a sweeping pattern from the LSB to the MSB, about twice per second. Between the sweep cycles, all LED positions shall be off.
5	Reset Button	
5.1	Press the Reset Button, A1S140.	For about 1 to 2 seconds, • Halt, LED131 – Red • Reset, LED132 – Yellow • Run, LED133 – Off
5.2	Wait for the reset operation to pass.	After the reset period, • Halt, LED131 – Off • Reset, LED132 – Off • Run, LED133 – Green
6	6800 Peripheral Support In the background for most tests, the program produces an ocean wave simulation sound effect via a MOS 6581 that is addressed to $00800000. This tests 6800 peripheral support.	
6.1	Connect the MOS 6581 as indicated in Appendix A.	Verify that the ocean wave simulation sound effects are generated.
7	On-Board Input Counter (Int 2) The digital input from the Clock Synchronization Register is used as the addend to advance the counter displayed. Bringing a Digital Input high advances the corresponding counter bit to advance. The inputs are the pins 6, 8, 10 and 12 from least to most significant bits.  	

7.1	Use a pull-up wire connected to MB68k-100 +5VDC to the trigger for Autovector Interrupt 2 at A1CON340, position 4.	Verify all LEDs on the On-Board Output Latch, DZ290, are off.
7.2	Use the pull-up wire to connect to only A1CON300, pin 12. This connection may be made repeatedly for additional test of the function.	Verify bits 3-7 of DZ290 cycle while the wire is connected. Bits 0-2 shall remain off.
7.3	Again, use the pull-up on pin 10.	Verify bits 2-7 of DZ290 cycle while the wire is connected. Bits 0 and 1 shall remain off.
7.4	Again, use the pull-up on pin 8.	Verify bits 1-7 of DZ290 cycle while the wire is connected. Bit 0 shall remain off.
7.5	Again, use the pull-up on pin 6.	Verify all bits of DZ290 cycle while the wire is connected.
8	SVS Input (Int 3) All four bytes retrieved from the SVS input are logical ORed together and displayed. Since bytes at addresses 0-7 except for 1 and 5 are all zero, the result should only reflect these two values. And reads from 1 and 5 match as the value read in from the SVS jumper selection. Therefore the only positions lit are those with jumpers installed.	
8.1	Remember the starting SVS jumper selection on the SVS Selector, A1JP180, in order to restore it after this test.	--
8.2	Use the pull-up at A1CON340, position 5.	--
8.3	Install only a single jumper on A1JP180 in each position from 1 through 8.	Verify that only the LED in the corresponding position on the On-Board Output Latch illuminates.
8.4	Restore the SVS jumper selection as installed prior to the test.	--

<table>
<tr><td>9</td><td colspan="2">Hardware Entropy Generator (Int 4)
This test is intended to be done in conjunction with hardware tests for suitable randomness. Output is gathered from the Hardware Entropy Generator, and an average is calculated from this output. The average is displayed as a fractional part on the On-Board Output Latch. Balance is observed as an absolute value around $80. Variability is observed with the value also showing some dynamic variation. The average is continually displayed as it is calculated over 65536 samples. Between cycles, all lights illuminate for about a second, and the average calculation is reset.
 
</td></tr>
<tr><td>9.1</td><td>Use the pull-up at A1CON340, position 6.</td><td>--</td></tr>
<tr><td>9.2</td><td>Monitor the On-Board Output Latch between cycle resets. Cycle resets are indicated by all Output Latch LEDs illuminating together for about 1 second. Between those, the cumulative average of the output is displayed.</td><td>Verify the displayed value suitably approaches $80 and demonstrates sufficient variability. Full test of the Hardware Entropy Generator shall have been done during assembly by confirming waveforms with an oscilloscope.</td></tr>
<tr><td>10</td><td colspan="2">Bank 0 SRAM (Int 5)
This test cycles through 32kB of Bank 0 memory space, writing the location’s own address to each byte in memory with an incrementing bit flip pattern. At the start of each pass through memory, this Exclusive-OR flip pattern value that is used against the address is briefly flashed on the display. A failure to read back the correct value written in SRAM then signals an LED to light on the display. This state is maintained across flashes of the flip pattern, thus indicating where a fault has occurred. Each bit represents a memory range and odd/even position. Note that memory references alias past the size of the physical SRAM, so memory may be scanned multiple times in one pass and a failure may be indicated in an aliased address.

Bit 0 - LSB (Hi), < 8kB
Bit 1 - LSB (Hi), < 16kB
Bit 2 - LSB (Hi), < 32kB
Bit 3 - LSB (Hi), < 64kB
Bit 4 - MSB (Lo), < 8kB
Bit 5 - MSB (Lo), < 16kB
Bit 6 - MSB (Lo), < 32kB
Bit 7 - MSB (Lo), < 64kB</td></tr>
</table>

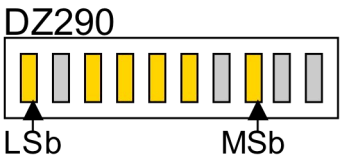
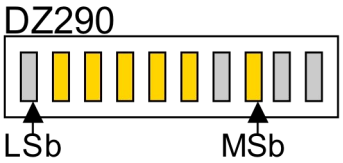
10.1	Use the pull-up at A1CON340, position 7.	Verify that no On-Board Output Latch LEDs illuminate steadily within the span of installed SRAM memory, as described above.
10.2	The test may be left to run until the flashing flip pattern completes a full 8-bit cycle.	Continue verifying that no On-Board Output Latch LEDs illuminate within the span of installed SRAM memory, as described above.
11	Interrupt Enable Mask (Int 6) This test verifies the global and individual enable masks of the Interrupt Logic. The LED position lit indicates the interrupt level suppressed. To test, trigger the corresponding interrupt. In this test, the function of the interrupt shall be suppressed, and thus the test mode shall not change. In the first state with all 7 LEDs lit, the global mask is tested. The test shall advance automatically through each state to test each masking case. When complete, all lights are off. At this time, the test mode may be changed by triggering an interrupt as normal.	
11.1	Use the pull-up at A1CON340, position 8.	Verify that LEDs for bits 0-6 illuminate.
11.2	With bits 0-6 illuminated, connect A1CON340 pins 3 through 9 each with the pull-up wire.	Verify that the bits 0-6 remain illuminated for 15 seconds since entering this test mode. The mode shall not change due to connection with the pull-up wire.
11.3	Wait for only bit 0 to remain illuminated on the On-Board Output Latch.	Verify that the On-Board Output Latch transitions to only bit 0 illuminated.
11.4	While only bit 0 is lit, connect the pull-up to A1CON340, position 3.	Verify, while only bit 0 is lit, that the mode does not change by connecting position 3.
11.5	Repeat this sequence of testing for each of pins 4 through 9 on A1CON340, as the On-Board Output Latch cycles through bits 1 through 6.	Verify, while the corresponding bit is lit, that the mode does not change by connecting the pull-up.

12	Select and Acknowledge Logic (Int 7) In this mode memory reads are executed from each Block Address. With the Bus Error Timer disabled, execution freezes until Auto /DTACK is installed for the pending Block Address. During this time the Halt, Reset and Run LEDs shall all be off. Installing Auto /DTACK for each Block Address in succession allows execution to proceed until the next open Auto /DTACK Block Address is encountered. Execution continues for about a second for each Block Address before the next block is addressed. The pending Block Address is indicated by the corresponding illuminated LED being displayed. Enabling the Bus Error Timer shall result in the display showing $BE, indicating a Bus Error has been encountered.  	
12.1	Remove A1JP331 to disable the Bus Error Timer.	--
12.2	Use the pull-up at A1CON340, position 9.	Observe bit 0 of the On-Board Output Latch briefly illuminates.
12.3	Wait for bit 1 of the On-Board Output Latch to illuminate.	Verify the Halt, Reset and Run lights are all off.
12.4	Momentarily install a shorting jumper in A1JP250 at position 2.	Verify that the Run light illuminates briefly and that the On-Board Output Latch advances to bit 2.
12.5	Repeat for positions 3-7 for bits 3-7.	Verify operation in the manner of the previous step for each position.
12.6	Repeat for position 8.	Verify the On-Board Output Latch bit advances around to position 1.
12.7	Reinstall A1JP331 to enable the Bus Error Timer.	Verify • On-Board Output Latch indicates $BE • Halt, LED131 – Off • Reset, LED132 – Off • Run, LED133 – Off
12.8	Press the Reset Button, A1S140.	Verify that the system returns to the On-Board Register Initialization test.

13	/DTACK Source and Wait State Generator This is used to test the Wait State Generator. The Wait State Generator is set to introduce wait states, in order to observe slowed program execution. The external DTACK input is also verified.	
13.1	Remove the shorting jumper from A1JP260 and place it in position 8.	--
13.2	Press the Reset Button, A1S140.	Upon resumption of the program, verify execution of the On-Board Register Initialization test appears slowed.
13.3	Remove the A1JP260 jumper and shift it by one into each position until position 2. For each position, reset.	Verify that execution appears to speed up for each jumper position until position 2.
13.4	Move the A1JP260 jumper to position 2 and reset.	Verify • Halt, LED131 – Red • Reset, LED132 – Off • Run, LED133 – Off
13.5	Temporarily install a jumper between A1CON160/162, pin 5 (M68K_/AS) and A1CON160/162, pin 11 (/DTACK_EXT). Reset.	Verify that the system returns to the On-Board Register Initialization test at full speed.
13.6	Remove the temporary jumper and install the shorting jumper on to A1JP260, position 1. Reset.	Verify that the system returns to the On-Board Register Initialization test.
14	Shifting Counter (Int 1) A 32-bit counter is incremented and an 8-bit window of the counter is displayed. The position of the 8-bit window starts from the LSB and moves back and forth along the length of the 32-bit counter. This burn-in test allows for monitoring long-term operation.	
14.1	Use the pull-up at A1CON340, position 3.	Verify that the On-Board Output Latch begins displaying the 8-bit window of the 32-bit counter.
14.2	Allow system to run as a burn-in period.	Verify continued proper operation.

Troubleshooting:

- See also software errata section in TstExamp source code, as needed.
- Ensure all chips are properly inserted into the sockets, particularly the 68000.
- If the Halt and Reset LEDs remain illuminated, ensure sufficient input voltage is applied to allow the Discrete Voltage Supervisor to release the system from reset. Vcc should be +5VDC and a +4.90V typical absolute minimum relative to GND.
- Numerous system faults are trapped by 68000 interrupts. In the event that a fault interrupt occurs, a distinguishing value is displayed on the On-Board Output and processor execution is halted with the STOP instruction. Only the Power LED remains illuminated. The Bus Error, with value $BE displayed, is the one exception. With a Bus Error, the Halt and Power LEDs may illuminate.

Value	On-Board Output Depiction
$BD	
$BE	

Value	Handler Label	Fault Description
$BE	HNLR_BUSERR	Bus Error
$BB	HNLR_ADDRERR	Address Error
$B1	HNLR_ILLINSTR	Illegal Instruction
$B0	HNLR_ZERODIV	Zero Divide
$BC	HNLR_CHK	CHK Instruction
$B2	HNLR_TRAPV	TRAPV Instruction
$B3	HNLR_PRIVERR	Privilege Violation
$B4	HNLR_TRACE	Trace
$BA	HNLR_EMU1010	Line 1010 Emulator
$BF	HNLR_EMU1111	Line 1111 Emulator
$B5	HNLR_UNINT	Uninitialized Interrupt Vector
$B6	HNLR_SPURINT	Spurious Interrupt
$BD	HNLR_BADEXCPT	other exception

Appendix A: SID Connections